UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/827,184	04/19/2004	Anthony M. Chiu	00-C-016D1 (STMI01-00097)	2439

30425 7590 05/24/2005

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/827,184	CHIU, ANTHONY M.
	Examiner	Art Unit
	Khiem D. Nguyen	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The preliminary amendment filed on April 19th, 2004 has been entered.

Information Disclosure Statement

The Information Disclosure Statement filed on April 19th, 2004 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

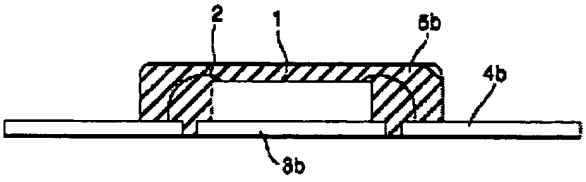
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 9-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii (U.S. Patent 5,835,988).

In re claim 9, **Ishii** discloses an integrated circuit package, comprising: an integrated circuit die **1** mounted on a lead frame **3b** including one or more leads or pins **4b**; and a plastic or epoxy material **5b** encapsulating at least part of the integrated circuit die **1** and a portion of the lead frame **3b** (col. 4, lines 27-60 and FIG. 4),

FIG. 4



wherein a portion of the lead frame remaining unencapsulated **4b** by the plastic or epoxy material **5b** is folded around sides of the encapsulated integrated circuit die **1** and over or adjacent to a peripheral upper surface of the plastic or epoxy material **5c** (col. 4, lines 60 to col. 5, line 11 and FIGS. 5-6).

FIG. 5

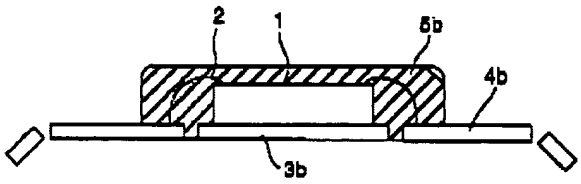
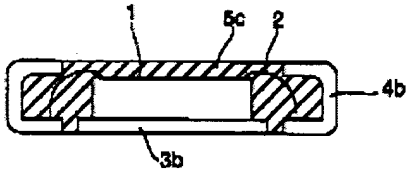


FIG. 6



In re claim 10, **Ishii** discloses that the integrated circuit package of claim 9, further comprising: a connection between a ground voltage and the portion of the lead frame folded around the sides of the encapsulated integrated circuit die and over or adjacent to the peripheral upper surface of the plastic or epoxy material (FIG. 6).

In re claim 11, **Ishii** discloses that the plastic or epoxy material **5b** encapsulates exposed surfaces of the integrated circuit die **1**, except for a sensing surface, and wire bonds **2** connecting the integrated circuit die **1** to portions of the lead frame **4b** (col. 4, lines 42-47 and FIG. 6).

In re claim 12, **Ishii** discloses that the portions of the lead frame **4b** are folded around each side of the encapsulated integrated circuit die **1** (col. 4, lines 62-66 and FIG. 6).

In re claim 13, **Ishii** discloses that a first portion of the lead frame folded around a first side of the encapsulated integrated circuit die includes an opening providing access for a connector to pins electrically connected to the integrated circuit die (FIG. 6).

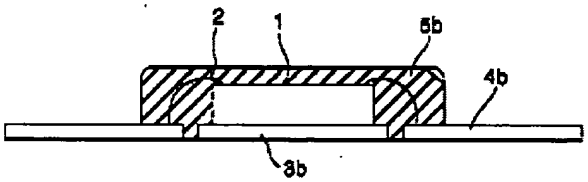
In re claim 14, **Ishii** discloses that the portions **4b** of the lead frame are folded only around edges of the encapsulated integrated circuit die **1** not including leads electrically connected to the integrated circuit die (FIG. 6).

In re claim 15, **Ishii** discloses that a first portion of the lead frame is folded around a side of the encapsulated integrated circuit die; and a second portion of the lead frame extending from the first portion is folded over a peripheral upper surface of the encapsulated integrated circuit die (FIG. 6).

In re claim 16, **Ishii** discloses that a first portion of the lead frame is folded around a side of the encapsulated integrated circuit die; and a second portion of the lead frame extending from the first portion is folded adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die (FIG. 6).

In re claim 17, **Ishii** discloses an integrated circuit package, comprising: a lead frame including a die paddle **3b**, one or more leads or pins **4b**, and portions extending from the die paddle; an integrated circuit die **1** mounted on the die paddle **3b** (col. 4, lines 22-60 and FIG. 4);

FIG. 4



a plastic or epoxy material **5b** encapsulating exposed surfaces of the integrated circuit die **1** except for a sensing surface,

wherein the portions of the lead frame **4b** extending from the die paddle **3b** are folded around sides of the encapsulated integrated circuit die **1** and over or adjacent to peripheral upper surfaces of the encapsulated integrated circuit die (col. 4, line 60 to col. 5, line 11 and FIG. 5-6).

FIG. 5

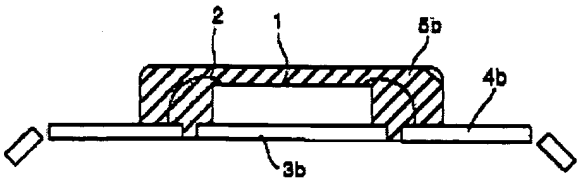
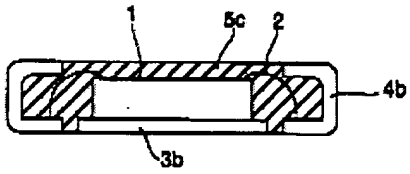


FIG. 6

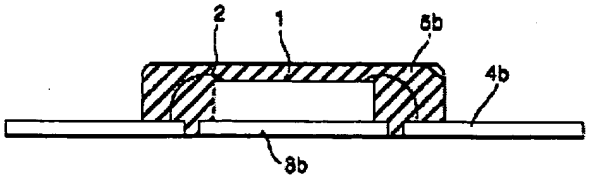


In re claim 18, **Ishii** discloses that the portions extending from the die paddle **3b** include openings around the pins or leads **4b** (FIG. 4).

In re claim 19, **Ishii** discloses that the portions extending from the die paddle **3b** project from peripheral edges of the die paddle not adjacent to the pins or leads (FIG. 6).

In re claim 20, **Ishii** discloses that a lead frame strip for an integrated circuit package, comprising: at least one lead frame, the lead frame including: a die paddle **3b** on which an integrated circuit **1** will be mounted; a plurality of structures which will be formed into pins or leads for the integrated circuit package (col. 4, lines 27-60 and FIG. 4); and

FIG. 4



portions extending from the die paddle **3b** which will be folded around sides of the integrated circuit package **1** and over or adjacent to a peripheral upper surface of the integrated circuit package to form an electrostatic discharge ring (col. 4, line 60 to col. 5, line 11 and FIG. 5-6).

FIG. 5

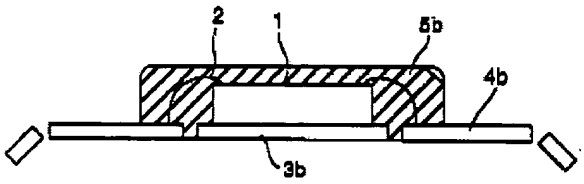
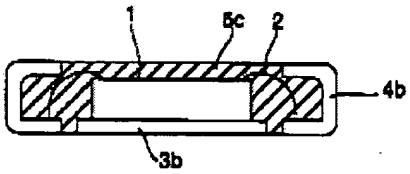


FIG. 6



2. Alternatively, claims 9, 17, and 20 are further rejected under 35 U.S.C. 102(b) as being anticipated by Culnane et al. (U.S. Patent 5,744,863).

In re claim 9, **Culnane** discloses an integrated circuit package, comprising: an integrated circuit die **150** mounted on a lead frame including one or more leads or pins **156**; and a plastic or epoxy material **162, 164** encapsulating at least part of the integrated circuit die **150** and a portion of the lead frame **156** (col. 4, lines 12-54 and FIG. 2),

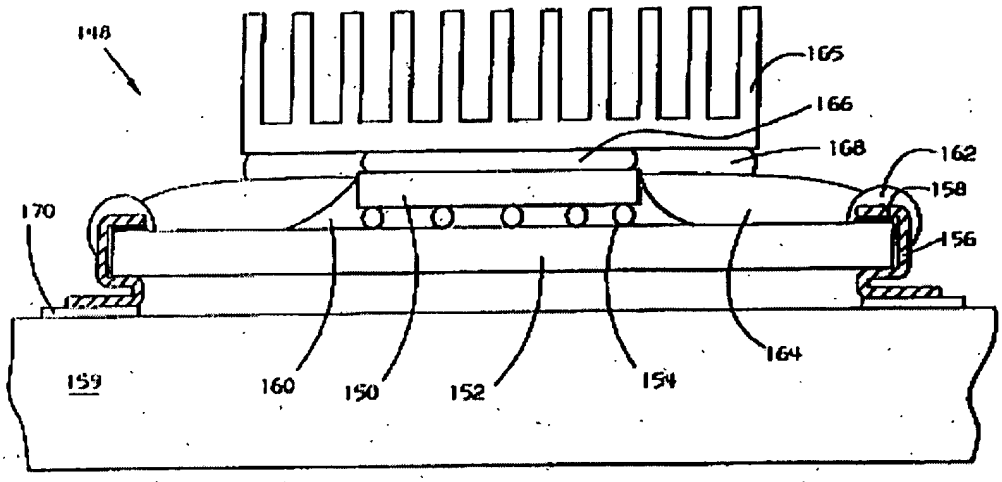


FIG. 2

wherein a portion of the lead frame remaining unencapsulated **156** by the plastic or epoxy material **162, 164** is folded around sides of the encapsulated integrated circuit die **150** and over or adjacent to a peripheral upper surface of the plastic or epoxy material (col. 4, lines 12-54 and FIG. 2).

In re claim 17, **Culnane** discloses an integrated circuit package, comprising: a lead frame including a die paddle **152**, one or more leads or pins **156**, and portions extending from the die paddle; an integrated circuit die **150** mounted on the die paddle (col. 4, lines 12-54 and FIG. 2);

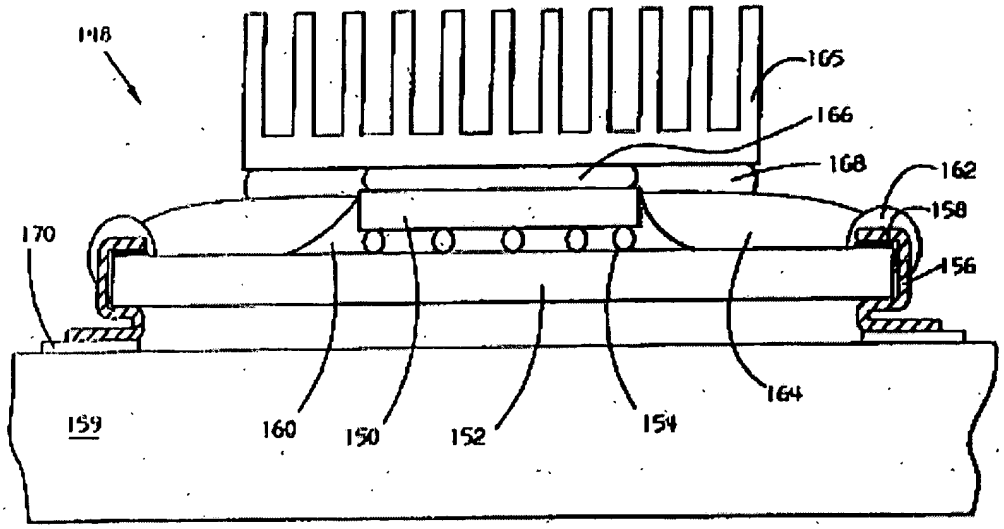


FIG. 2

a plastic or epoxy material **162, 164** encapsulating exposed surfaces of the integrated circuit die **150** except for a sensing surface,

wherein the portions **156** of the lead frame extending from the die paddle **152** are folded around sides of the encapsulated integrated circuit die **150** and over or adjacent to peripheral upper surfaces of the encapsulated integrated circuit die (col. 4, lines 12-54 and FIG. 2).

In re claim 20, **Culnane** discloses that a lead frame strip for an integrated circuit package, comprising: at least one lead frame, the lead frame including: a die paddle **152** on which an integrated circuit **150** will be mounted; a plurality of structures which will be formed into pins or leads **156** for the integrated circuit package (col. 4, lines 12-54 and FIG. 2); and

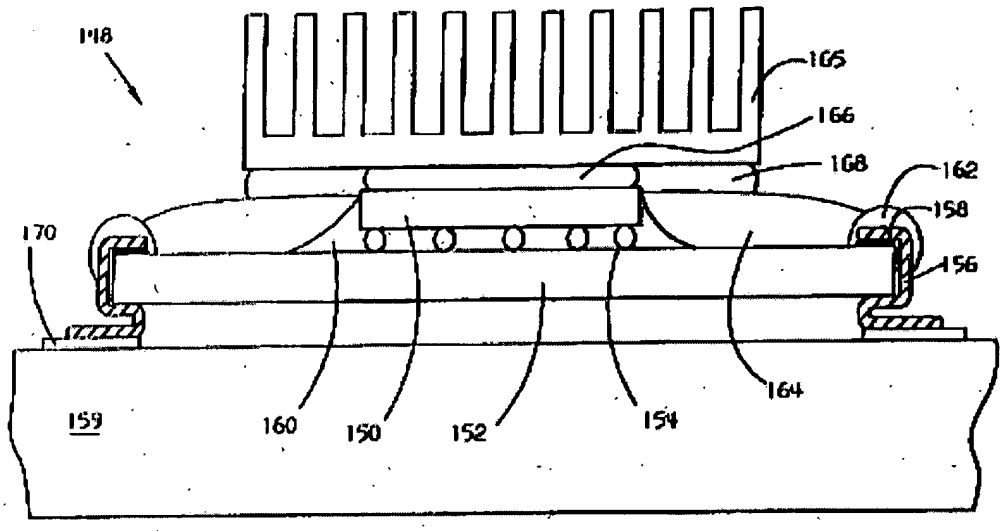


FIG. 2

portions **156** extending from the die paddle **152** which will be folded around sides of the integrated circuit package and over or adjacent to a peripheral upper surface of the integrated circuit package to form an electrostatic discharge ring (col. 4, lines 12-54 and FIG. 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
May 13th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER